Abraham Gonzalez

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Education

University of California, Berkeley Expected July 2025
Ph.D. in Electrical Engineering and Computer Sciences, advised by Krste Asanović, GPA: 3.96/4.0
Dissertation Title: "End-to-end Heterogeneous System Design for Hyperscale Big Data Processing"

The University of Texas at Austin August 2014 - May 2018
B.S. in Electrical and Computer Engineering, GPA: 3.98/4.0

Work Experience

Graduate Student Researcher August 2018 - Present
University of California, Berkeley — Berkeley, CA

- Advised by Professor Emeritus and Professor of the Graduate School Krste Asanović.
- Ph.D. candidate and ADEPT/SLICE lab member researching hyperscale cloud architectures, accelerator scheduling, and hardware design methodologies.
- Co-lead of the Hyperscale system-on-chip (SoC) project focused on hyperscale hardware/software co-design.
- Co-lead of the Chipyard SoC framework (used in 20+ tape-outs and 150+ pubs. @ 65+ companies/universities).
- Co-lead of the award-winning FireSim FPGA-accelerated simulator (used in 60+ pubs. @ 25+ companies/universities).
- Developer of the Berkeley Out-of-Order Machine (BOOM), the first open-source RISC-V out-of-order core.
- Led the tape-out/bring-up of the first Chipyard test chip, a 106.1 GOPS/W heterogeneous SoC in Intel 22FFL.
- Published research and tape-outs at top conferences including ISCA, DAC, IEEE MICRO, and ESSCIRC.
- Lead organizer for 10+ tutorials and workshops with 200+ unique attendees at top conferences.

Student Researcher Intern June 2021 - July 2024
Google — Sunnyvale, CA

- Student researcher working with Parthasarathy Ranganathan (Vice President and Engineering Fellow).
- Collaborated with the SystemsResearch@Google (SRG) and Systems Infrastructure Performance teams.
- Researched data processing and remote procedure call (RPC) optimizations as part of the Hyperscale SoC project.
- Published first of its kind research on hyperscale big data processing characterization at ISCA '23.
- Open-sourced HyperRPCBench, a novel representative RPC benchmark suite, with the Fleetbench team.

Silicon Engineering Group Intern June 2020 - August 2020
Apple — Cupertino, CA

- Engineering intern working with Si-En Chang (Distinguished Engineer).
- Developed computer architecture tooling for CPU verification.

Scalable Performance CPU Development Group Intern May 2018 - August 2018
Intel — Austin, TX

- Worked on debugging tools for the microcontroller integration team with senior engineers.
- Setup novel workflows and infrastructure between the firmware and microcontroller integration teams for agility.

Office Shared Graphics Explore Intern May 2016 - August 2016
Microsoft — Redmond, WA

- Developed the proof-of-concept "Sketchy Lines" feature (now publicly available) in the Office suite using C++.
- Investigated and coordinated new feature sets with senior engineers, program managers, and customers.

UIM Driver Intern May 2015 - August 2015
Qualcomm — San Diego, CA

- Designed a software framework for smartcard (UIM) interaction in C++/CLI and C++ with senior engineers.
- Integrated designed framework into a .NET application managing smartcards via CCID.

Skills

Programming Languages
Scala, C/C++, Python, Chisel, SQL, {System}Verilog, RISC-V, Bash, Make, Bazel, TCL, TensorFlow, PyTorch

Other
Git, MapReduce, AWS, Google Cloud, Xilinx Virtex/UltraScale+ FPGAs, Cadence EDA tooling

Honors, Awards, and Selections

UC Berkeley: DARPA Riser (Fa'22), Analog Devices Outstanding Designer (Sp'20), Berkeley Fellowship (Fa'18), EECS Excellence Award (Fa'18), GEM Fellowship (Sp'18), NSF GRFP Honorable Mention (Sp'18)
UT Austin and prior: Highest Honors (Sp'18), Distinguished College Scholar (Sp'17/18), College Scholar (Sp'16), Roberto Rocca Scholarship (Fa'17), Victor L. Hand Scholarship (Fa'16), TI Diversity Scholarship (Fa'15), 2nd Best Poster SHPE National Conference (Fa'17), Qualcomm DECA Attendee (1/51 selected nationally) (Sp'15), EOE/SHPE Freshman Academic Excellence Winner (Sp'15)