

# Abraham Gonzalez

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## Education

### University of California, Berkeley

Expected July 2025

*Ph.D. in Electrical Engineering and Computer Sciences*, advised by Krste Asanović, GPA: 3.96/4.0

Dissertation Title: “End-to-end Heterogeneous System Design for Hyperscale Big Data Processing”

### The University of Texas at Austin

August 2014 - May 2018

*B.S. in Electrical and Computer Engineering*, GPA: 3.98/4.0

## Job Experience

### Graduate Student Researcher

August 2018 - Present

University of California, Berkeley — Berkeley, CA

- Advised by Professor Emeritus and Professor of the Graduate School Krste Asanović.
- Ph.D. candidate and [ADEPT/SLICE lab](#) member researching hyperscale cloud architectures, accelerator scheduling, and hardware design methodologies.
- Co-lead of the [Hyperscale system-on-chip \(SoC\) project](#) focused on hyperscale hardware/software co-design.
- Co-lead of the widely used [Chippyard SoC framework](#), which has been used in over 20 tape-outs at multiple academic institutions and has been used (not only cited) by over 150 peer-reviewed publications from first authors at over 65 companies and academic institutions.
- Co-lead of the award-winning [FireSim FPGA-accelerated simulation platform](#), which has been used (not only cited) in over 60 peer-reviewed publications from first authors at over 25 companies and academic institutions.
- Led the tape-out and bring-up of the first [Chippyard](#) test chip, a 106.1 GOPS/W heterogeneous multi-core multi-accelerator SoC made in Intel 22FFL.
- Developer of the [Berkeley Out-of-Order Machine \(BOOM\)](#), the first open-source Linux-booting synthesizable and parameterizable RV64GC RISC-V out-of-order core.
- [Published research](#) and [tape-outs](#) at top conferences including ISCA, DAC, IEEE MICRO, and ESSCIRC.
- Lead organizer for [over 10 tutorials and workshops](#) with over 200 unique attendees at top conferences.
- Mentored over 10 graduate and undergraduate students in hyperscale systems and hardware methodology research.

### Student Researcher Intern

June 2021 - July 2024

Google — Sunnyvale, CA

- Student researcher working with Parthasarathy Ranganathan (Vice President and Engineering Fellow).
- Collaborated with the [SystemsResearch@Google \(SRG\)](#) and Systems Infrastructure Performance teams.
- Researched data processing and remote procedure call (RPC) optimizations as part of the [Hyperscale SoC project](#).
- Published research on [hyperscale big data processing characterization at ISCA '23](#).
- Open-sourced [HyperRPCBench](#), a novel representative RPC benchmark suite, with the [Fleetbench](#) team.

### Silicon Engineering Group Intern

June 2020 - August 2020

Apple — Cupertino, CA

- Engineering intern working with Si-En Chang (Distinguished Engineer).
- Developed computer architecture tooling for CPU verification.

### Scalable Performance CPU Development Group Intern

May 2018 - August 2018

Intel — Austin, TX

- Worked on debugging tools for the microcontroller integration team with senior engineers.
- Setup novel workflows and infrastructure between the firmware and microcontroller integration teams for agility.

### Office Shared Graphics Explore Intern

May 2016 - August 2016

Microsoft — Redmond, WA

- Developed the proof-of-concept “Sketchy Lines” feature (now publicly available) in the Office suite using C++.
- Investigated and coordinated new feature sets with senior engineers, program managers, and customers.
- Created a synchronized network of Arduino microcontrollers using HTTP requests for the OneWeek hackathon.

### UIM Driver Intern

May 2015 - August 2015

Qualcomm — San Diego, CA

- Designed a software framework for smartcard (UIM) interaction in C++/CLI and C++ with senior engineers.
- Integrated designed framework into a .NET application managing smartcards via CCID by utilizing APDU transmission/logging; file system viewing; file data parsing/manipulation; and smartcard reader management.
- Created gesture controlled car with Particle Core for the Hack-Mobile hackathon.

# Graduate Research Experience

## Hyperscale SoC Project

April 2019 - Present

University of California, Berkeley — Berkeley, CA

- Co-lead of the Hyperscale SoC project focused on developing next-generation hyperscale computing.
- Focused on hyperscale big data processing platforms and RPC accelerator scheduling research.
- Combines the use of [Chipyard](#) and [FireSim](#) to explore new hardware/software co-design opportunities for big data processing platforms.
- Characterized three big data processing platforms (Spanner, BigTable, and BigQuery), running live-traffic at Google for the first time and [published the work at ISCA '23](#).
- Collaborated with the [Fleetbench](#) benchmarking team to open-source [HyperRPCBench](#), a novel representative synthetic RPC benchmark suite including payloads and a traffic driver.
- Built and correlated Python and C++ models for accelerator runtimes against x86 proof-of-concepts and [Chipyard](#)-based RTL running custom and [HyperRPCBench](#) payloads.

## Chipyard: Agile RISC-V Hardware SoC Design Framework

April 2019 - Present

University of California, Berkeley — Berkeley, CA

- Co-lead and core developer of [Chipyard](#), an integrated agile RISC-V SoC design, simulation, and implementation environment for specialized compute systems.
- Architected the main integration, build flow, and repository structure.
- Added support for multiple IPs including [BOOM](#), [SiFive blocks](#), [Ariane \(CVA6\)](#), [NVDLA](#), and more.
- Integrated the initial tape-out bring-up tether widget, FPGA bring-up flow, and software utilities.
- Added the initial CI/CD flow including torture/fuzz and distributed testing.
- Used in [over 20 tape-outs](#) at multiple academic institutions (such as Stanford and Technical University of Dresden).
- Used (not only cited) in [over 150 peer-reviewed publications](#) (spanning computer architecture, artificial intelligence (AI), systems, and more) from first authors at over 65 companies and academic institutions.
- [Over 650 unique forks and 1.8K stars on GitHub](#).

## FireSim: FPGA-accelerated Hardware Simulation Platform

August 2018 - Present

University of California, Berkeley — Berkeley, CA

- Co-lead and core developer of [FireSim](#), an FPGA-accelerated full-system hardware simulation platform with on-premises and cloud flexibility.
- Added FPGA-accelerated co-simulation with [Dromajo](#), enabling bug discovery billions of cycles into simulation.
- Re-architected the command-line interface and Python machine manager to support configurable custom clusters.
- Enabled larger simulations through local FPGA support with [U250/U280/U200](#) Xilinx UltraScale+ FPGAs and the [Xilinx Vitis Unified Software Platform](#).
- Expanded the initial CI/CD flow to include FPGA bitstream builds and simulations across local and cloud FPGAs.
- Used (not only cited) in [over 60 peer-reviewed publications](#) from first authors at over 25 companies and academic institutions in addition to being used in the development of commercial chips.
- Used as a [standard host platform for DARPA and IARPA programs](#), including in [DARPA's first ever bug bounty program \(FETT\)](#) to host novel security-augmented hardware designs on the internet for attack by 100s of white-hat hackers across the globe.
- [Over 200 unique forks and 900 stars on GitHub](#).

## BEAGLE: Heterogeneous Multi-Core Multi-Accelerator Tape-out in Intel 22FFL

April 2019 - September 2021

University of California, Berkeley — Berkeley, CA

- Led tape-out of the first [Chipyard](#) test chip, a 106.1 GOPS/W heterogeneous multi-core multi-accelerator test chip made in Intel 22FFL.
- Coordinated interaction between UC Berkeley and Intel during physical design process.
- Streamlined [Chipyard](#) vendor IP integration and custom boot flow.
- Led bring-up including open-sourcing newly created FPGA-based bring-up collateral.
- Led pre-silicon testing with large-scale [FireSim](#) simulations and automated [Chipyard](#) regressions.
- [Published working test chip at ESSCIRC '21](#).
- SoC Components: [In-order Rocket core](#) with a [Gemmini systolic array accelerator](#), [out-of-order BOOM core](#) with a [Hwacha vector accelerator](#) and runtime configurable non-speculative mode, [shared L2](#), independent clock domains, and [multiple IOs \(GPIO, SPI, I2C, UART, SerDes\)](#).

## BOOM: The Berkeley Out-of-Order Machine

August 2018 - April 2021

University of California, Berkeley — Berkeley, CA

- Developer of BOOM, the first open-source synthesizable Linux-booting RV64GC RISC-V out-of-order core.
- Added the initial CI/CD flow including torture/fuzz and distributed testing.
- Modified the RTL to support instantiation with other core IPs in addition to various quality-of-life improvements.
- [Open-sourced and replicated Spectre speculative attacks on the core](#).

# Skills

## Programming Languages —

- *Highly Proficient:*
  - Traditional: Scala, C, C++, Python, RISC-V Assembly, Bash, C++/CLI
  - Hardware Description/Construction Languages (HDL/HCLs): Chisel, SystemVerilog, Verilog
  - Scripting and build systems: Make, CMake, Bazel, TCL
  - Machine Learning: TensorFlow, PyTorch
  - Other: SQL
- *Proficient:*
  - Traditional: ARM Assembly, LC-3 Assembly, Android Java, C#
  - Hardware Description/Construction Languages (HDL/HCLs): VHDL

**Tooling** — Tiva Launchpad, Arduino, SparkFun, Particle Core microcontrollers

**Embedded Systems** — Tiva Launchpad, Arduino, SparkFun, Particle Core microcontrollers

**Electrical Equipment** — Soldering, oscilloscopes, logic analyzers, multimeters

**Other** — Git, MapReduce, AWS, Google Cloud, Xilinx Virtex/UltraScale+ FPGAs, Cadence EDA tooling

# Conference, Journal, Workshop, and Technical Report Publications

**Summary** (underline = first author or equal contribution)

ISCA '24, ISCA '23, ESSCIRC '21, ISPASS '21, DAC '20 (invited), IEEE Micro 2020.4, CARRV '20, UC Berkeley Technical Report '20, CARRV '19

**FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs** ISCA '24  
Joonho Whangbo, Edwin Lim, Chengyi Lux Zhang, Kevin Anderson, [Abraham Gonzalez](#), Raghav Gupta, Nivedha Krishnakumar, Sagar Karandikar, Borivoje Nikolić, Yakun Sophia Shao, Krste Asanović, “FireAxe: Partitioned FPGA-Accelerated Simulation of Large-Scale RTL Designs”, *2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA)*, Buenos Aires, Argentina, June 2024.  
Received all available artifact badges: Artifacts Available, Artifacts Evaluated: Functional, and Results Reproduced

**Profiling Hyperscale Big Data Processing** ISCA '23  
[Abraham Gonzalez](#), Aasheesh Kolli, Samira Khan, Sihang Liu, Vidushi Dadu, Sagar Karandikar, Jichuan Chang, Krste Asanović, Parthasarathy Ranganathan, “Profiling Hyperscale Big Data Processing”, *2023 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA)*, Orlando, FL, USA, June 2023.  
Received all available artifact badges: Artifacts Available, Artifacts Evaluated: Functional, and Results Reproduced

**A 16mm<sup>2</sup> 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET** ESSCIRC '21  
[Abraham Gonzalez](#), Jerry Zhao, Ben Korpan, Hasan Genc, Colin Schmidt, John Wright, Ayan Biswas, Alon Amid, Farhana Sheikh, Anton Sorokin, Sirisha Kale, Mani Yalamanchi, Ramya Yarlagadda, Mark Flannigan, Larry Abramowitz, Elad Alon, Yakun Sophia Shao, Krste Asanović, and Bora Nikolić, “A 16mm<sup>2</sup> 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET”, *In proceedings of 2021 IEEE European Solid State Circuits Conference (ESSCIRC 2021)*, Virtual Event, September 2021.

**COBRA: A Framework for Evaluating Compositions of Hardware Branch Predictors** ISPASS '21  
Jerry Zhao, [Abraham Gonzalez](#), Alon Amid, Sagar Karandikar, and Krste Asanović, “COBRA: A Framework for Evaluating Compositions of Hardware Branch Predictors”, *In proceedings of 2021 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2021)*, Virtual Event, March 2021.

**Invited: Chipyard - An Integrated SoC Research and Implementation Environment** DAC '20 (invited)  
Alon Amid, David Biancolin, [Abraham Gonzalez](#), Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Yakun Sophia Shao, Krste Asanović, and Bora Nikolić, “Invited: Chipyard - An Integrated SoC Research and Implementation Environment”, *In proceedings of 57th ACM/IEEE Design Automation Conference (DAC 2020)*, San Francisco, CA, USA, July 2020.

**Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs** IEEE Micro 2020.4  
Alon Amid, David Biancolin, [Abraham Gonzalez](#), Daniel Grubb, Sagar Karandikar, Harrison Liew, Albert Magyar, Howard Mao, Albert Ou, Nathan Pemberton, Paul Rigge, Colin Schmidt, John Wright, Jerry Zhao, Yakun Sophia Shao, Krste Asanović, and Bora Nikolić, “Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs”, *IEEE Micro*, vol. 40, no. 4, pp. 10-21, (Special Issue on Agile and Open-Source Hardware), July-August 2020.

**SonicBOOM: The 3rd Generation Berkeley Out-of-Order Machine** CARRV '20  
Jerry Zhao, Ben Korpan, [Abraham Gonzalez](#), and Krste Asanović, “SonicBOOM: The 3rd Generation Berkeley Out-of-Order Machine”, *4th Workshop on Computer Architecture Research with RISC-V (CARRV 2020)*, Virtual Event, May 2020.

**A Chipyard Comparison of NVDLA and Gemmini** UC Berkeley Technical Report '20  
[Abraham Gonzalez](#), and Charles Hong, “A Chipyard Comparison of NVDLA and Gemmini”, *EECS Department*, University of California, Berkeley, May 2020.

**Replicating and Mitigating Spectre Attacks on an Open Source RISC-V Microarchitecture** CARRV '19  
[Abraham Gonzalez](#), Ben Korpan, Jerry Zhao, Ed Younis, and Krste Asanović, “Replicating and Mitigating Spectre Attacks on an Open Source RISC-V Microarchitecture”, *3rd Workshop on Computer Architecture Research with RISC-V (CARRV 2019)*, Phoenix, AZ, USA, June 2019.

## Selected External Presentations

**End-to-end Heterogeneous System Design for Hyperscale Big Data Processing** April 2025  
Google — Sunnyvale, CA

**End-to-end Heterogeneous System Design for Hyperscale Big Data Processing** April 2025  
Apple — Cupertino, CA

**Chipyard: An Open-Source RISC-V SoC Design Framework** April 2023  
Latch-Up Conference — Santa Barbara, CA

**FireSim: Fast and Effortless FPGA-accelerated Hardware Simulation with On-Prem and Cloud Flexibility** March 2023  
Apple — Cupertino, CA

**A 16mm<sup>2</sup> 106.1 GOPS/W Heterogeneous RISC-V Multi-Core Multi-Accelerator SoC in Low-Power 22nm FinFET** September 2021  
ESSCIRC — Virtual

**Chipyard: Integrated SoC Design, Simulation, Implementation Environment** July 2020  
Apple — Virtual

**End-to-End Architecture Exploration with RISC-V SoC Generators, FPGA-Accelerated Simulation and Agile Test Chips** December 2019  
RISC-V Summit — San Jose, CA

**Replicating and Mitigating Spectre Attacks on an Open Source RISC-V Microarchitecture** June 2019  
CARRV — Phoenix, AZ

**The Berkeley Out-of-Order Machine: An Open-Source Synthesizable High-Performance RISC-V Processor** May 2019  
Latch-Up Conference — Portland, OR

**Enhancing an Out-of-Order Processor Simulator for Cloud Applications** May 2018  
Capstone Presentation at The University of Texas at Austin — Austin, TX

**A Machine Learning Approach to Modeling Electroplating Process Variations in IC Redistribution Layers** November 2017  
SHPE National Conference — Kansas City, MO

## Tutorials and Workshops Organized

**Full-day Hands-on Tutorials on FireSim and Chipyard**  
[MICRO '24](#), [ISCA/ASPLOS/HPCA '23](#), [ISCA/MICRO/ASPLOS '22](#), [ISCA/MICRO '21](#), [MICRO '19](#)  
Lead organizer presenting a series of full-day, hands-on tutorials on the Chipyard SoC framework and the FireSim FPGA-accelerated simulation platform at ten recent conferences, supported by the NSF-CCRI program, AWS, and Xilinx. Over 200 unique attendees were provided free AWS EC2 instances to customize RTL and boot large-scale simulations (e.g., booting Linux, running AI workloads, etc.) using Chipyard, FireSim, and cloud FPGAs.

## First FireSim/Chippyard User and Developer Workshop

ASPLOS '23

Organizer of a full-day workshop consisting of 10 presentations from external users of the [Chippyard SoC framework](#) and the [FireSim FPGA-accelerated simulation platform](#), discussions on feature development, and discussions on open-source governance of the platforms.

## Undergraduate Research Experience

### Enhancing an Out-of-Order Processor Simulator for Cloud Applications

January 2018 - May 2018

The University of Texas at Austin — Austin, TX

- Undergraduate researcher working under [Professor Mattan Erez](#) for the UT Austin capstone design course.
- Designed and developed new software data-structures for emulating simultaneous multithreading on ZSim.
- Built hardware scheduling policies ensuring quality of service for latency critical tasks in an out-of-order pipeline.
- Presented a poster of final results at The University of Texas Electrical Engineering Spring Open House.

### Microsystems Technology Lab Intern

June 2017 - August 2017

Massachusetts Institute of Technology — Cambridge, MA

- Selected as one of 37 [MIT Summer Research Program \(MSRP\)](#) participants.
- Researched variations in electroplating growth in redistribution layers under [Professor Duane Boning](#).
- Designed various neural networks and machine learning models for electroplating growth using Tensorflow.
- Awarded 2<sup>nd</sup> best research poster at the SHPE National Conference '17 for research presented.

### Printing Electronics Research Assistant

January 2017 - June 2017

The University of Texas at Austin — Austin, TX

- Researched and fabricated printed antennas under the supervision of [Professor Ray Chen](#).
- Printed and tested fixed phase array antennas on Kapton with various nano-particle inks.

### QCA Research Assistant

May 2015 - August 2016

The University of Texas at Austin — Austin, TX

- Researched and designed quantum cellular automata (QCA) circuitry with [Professor Earl Swartzlander](#).
- Optimized QCA implementations of the carry-lookahead and conditional sum adders through QCA Designer.

## Teaching Experience

### Teaching Assistant - CS152/252A: Computer Architecture and Engineering

Spring 2023

University of California, Berkeley — Berkeley, CA

- Taught one discussion section per week in addition to developing new homework, tests, and labs.

### Head Teaching Assistant - EE290-2: Hardware for Machine Learning

Spring 2021

University of California, Berkeley — Berkeley, CA

- Taught one discussion section per week in addition to developing new homework, tests, and labs.

### Teaching Assistant - EE460N/382N.1: Computer Architecture

Spring 2018

The University of Texas at Austin — Austin, TX

- Taught two discussion sections per week in addition to developing new homework, tests, and labs.

### Tutor - Equal Opportunity in Engineering

Spring 2018

The University of Texas at Austin — Austin, TX

- Assisted struggling students in electrical and computer engineering courses through tailored guides and lessons.

## Professional Leadership and Extracurriculars

**Member** — Latinx Association of Graduate Students in Engineering and Science

Fall 2018 - Present

**Member** — Diversifying Future Leadership in the Professoriate (FLIP) Alliance

Fall 2018 - Present

**Vice President** — Eta Kappa Nu Electrical Engineering Honor Society

Fall 2017 - Spring 2018

**Corresponding Secretary** — Eta Kappa Nu Electrical Engineering Honor Society

Summer 2017 - Fall 2017

**Member** — Eta Kappa Nu Electrical Engineering Honor Society

Spring 2016 - Present

**Member** — Institute of Electrical and Electronic Engineers

Fall 2014 - Present

**Member** — Society of Hispanic Professional Engineers (SHPE)

Fall 2014 - Present

**Pi Tutor** — Equal Opportunity in Engineering (EOE)

Fall 2015, Fall 2017

**Academic Director** — Society of Hispanic Professional Engineers

Summer 2016 - Summer 2017



**Organizing Committee Member** — 3 Day Startup Austin  
**Participant** — 3 Day Startup Austin

Fall 2014 - Fall 2015  
Fall 2014

## Honors, Awards, and Selections

<b>DARPA Riser</b> — DARPA	Fall 2022
<b>Analog Devices Outstanding Engineer Award</b> — University of California, Berkeley	Spring 2020
<b>EECS Excellence Award</b> — University of California, Berkeley	Fall 2018
<b>Berkeley Fellowship for Graduate Study</b> — University of California, Berkeley	Fall 2018
<b>GEM Fellowship Recipient</b> — GEM	Spring 2018
<b>Honorable Mention</b> — NSF GRFP	Spring 2018
<b>Highest Honors</b> — The University of Texas at Austin	Spring 2018
<b>Distinguished College Scholar</b> — The University of Texas at Austin	Spring 2018
<b>Academic Leader Hall of Fame Inductee</b> — Equal Opportunity in Engineering Program	Spring 2018
<b>Roberto Rocca Scholarship Recipient</b> — Tenaris	Fall 2017
<b>Second-Place Award Winner</b> — SHPE National Conference Poster Competition	Fall 2017
<b>Distinguished College Scholar</b> — The University of Texas at Austin	Spring 2017
<b>Victor L. Hand Scholarship Recipient</b> — Victor L. Hand Endowed Scholarship Fund	Fall 2016
<b>College Scholar</b> — The University of Texas at Austin	Spring 2016
<b>Diversity Scholarship Recipient</b> — Texas Instruments	Fall 2015
<b>Freshman Academic Excellence Award Winner</b> — EOE and SHPE	Spring 2015
<b>Qualcomm DECA Attendee - selected as 1 of 51 nationally</b> — Qualcomm	Spring 2015
<b>LEAD Conference Attendee - selected as 1 of 30 nationally</b> — LEAD	Summer 2013

## References

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